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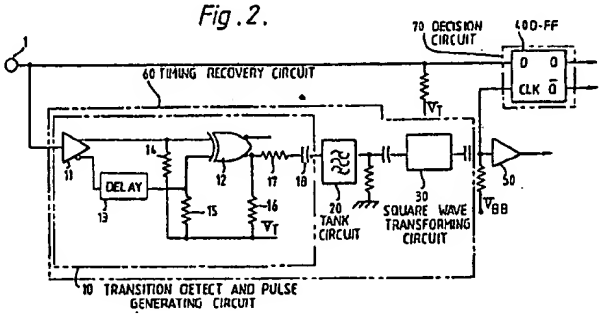
(54) Digital signal regenerator.

(57) A digital signal regenerator responsive to a data bit stream having a predetermined bit rate for generating a retimed data bit stream includes a transition detector and a pulse generator responsive to the data bit stream for detecting transition positions between two different states of the data bit stream and for generating width variable pulses at the transition positions, a filter responsive to the width variable pulses for extracting a timing wave of the data bit stream, a clock pulse generator responsive to the timing wave for generating a clock pulse sequence, and a discriminator responsive to the clock pulse sequence for discriminating the levels "1" and "0" of the data bit sequence to generate the retimed data bit stream.

Fig.2.



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Description

DIGITAL SIGNAL REGENERATOR

BACKGROUND OF THE INVENTION

This invention relates to a digital signal regenerator which regenerates a high bit rate digital signal received from a transmission line, and more particularly to a regenerator having an improved timing recovery circuit which extracts a timing wave from the received signal.

Fiber optic digital transmission systems have tremendous capacity to transmit large amounts of information over a single optical fiber and provide a very high bit rate digital transmission. However, as the bit rate increases, an improved timing recovery technique is required for accurate regeneration of the transmitted digital data.

As a prior art regenerator, Robert L. Rosenberg et al disclose a regenerator which is applicable at bit rates of 100 to 1000 Mbit/s and more in a paper entitled "Optical Fiber Repeatered Transmission Systems Utilizing SAW Filters" in IEEE Transactions on Sonics and Ultrasonics, Vol. 30, No. 3, pp. 119 - 126, May, 1983.

Figure 1 is a partial reproduction of the Rosenberg et al regenerator which receives a high bit rate data pulse stream, equalizes it with an equalizer 100, recovers a clock pulse stream with a timing recovery circuit 200, and regenerates the transmit pulse stream with a decision circuit 300 gated by the clock pulse stream. The timing recovery circuit 200 differentiates the received data pulse stream from the equalizer 100 with a prefilter 201 having differential characteristics to provide the transition points of the pulse stream. The differentiated pulse stream undergoes full-wave rectification with a rectifier 202, and the rectified pulse stream is fed to a filter 203 (SAW filter, for instance) which has bandpass characteristics and extracts timing wave whose frequency is twice the transmitted data bit rate when the transmitted data pulse stream has an NRZ (Non-return-to-zero) format. The timing wave is transformed into a square wave (timing clock stream) by a limit amplifier 204, and the phase of the timing clock stream is adjusted by a phase adjuster 205, and then supplied to the decision circuit 300 and other processing circuits. The decision circuit 300 comprises a simple digital circuit such as a D-type flip-flop, which samples the received data pulse stream coming from the equalizer 100 at the rise (or fall) of the pulses of the timing clock sequence from a phase adjuster 205, and regenerates the data pulse stream as a stream of well-shaped electrical data pulse stream having nearly constant amplitude and consistent timing of transitions. The phase adjuster performs a timing adjustment of the rise (or falls) positions of the clock pulses so that the clock pulse sequence drives the D-type flip-flop at center positions in time of individual received data pulses. The adjustment is requisite to control the decision errors which are otherwise caused by phase jitter contained in the received data pulse stream. These errors are generally likely to appear when the rise (or fall) positions in time of the received data pulse stream lies close to those of the clock pulses.

Assume a bit rate of 100 Mbit/s, the phase adjustment which is necessary to shift over a period of the data pulse is just 10 nsec in maximum. However, the phase adjuster involves a degradation of several nsec in the rise (or fall) of the timing clock due to the effect of bandwidth limitation, thus permissible time range for sampling the received data bit stream is limited only to several nano-seconds. This time limitation leaves no margin long enough to adjust the timing of clock to be applied to the decision circuit, resulting in decision errors. Moreover, when the degraded timing pulses having long rise or fall time drive the D-type flip-flop, the phase relation between the received data pulse stream and the clock pulse stream inconveniently varies, rendering the adjustment in phase relation extremely difficult.

SUMMARY OF THE INVENTION

An object of this invention is to provide a regenerator which can produce a regenerated data pulse stream with reduced decision errors.

Another object of the invention is to provide a regenerator which permits the use of a phase adjustable clock pulse sequence with no deterioration in rise and fall characteristics of recovered clock pulses.

Yet another object of the invention is to provide a regenerator which is adaptable to a high bit rate data pulse stream.

The regenerator according to this invention receives a data bit stream having a predetermined bit rate for generating a retimed data bit stream. The regenerator comprises transition detect and pulse generating means responsive to the data bit stream for detecting transition positions between two different states of the data bit stream and for generating width variable pulses at the transition positions, filtering means response to the width variable pulse for extracting a timing wave of the data bit stream, clock pulse generating means responsive to said timing wave for generating a clock pulse sequence, and discriminating means responsive to the clock pulse sequence for discriminating the levels "1" and "0" of the data bit sequence to generate the retimed data bit stream.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be better understood from the following detailed description if taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram to show a prior art digital signal regenerator;

FIG. 2 a block diagram to show an embodiment of this invention; and

FIGS. 3 and 4 waveform charts in main portions of the embodiment of FIG. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In FIG. 2, a digital signal regenerator of the present invention comprises a timing recovery circuit 60 and a decision circuit 70. The timing recovery circuit comprises a transition detect and pulse generating circuit 10 which detects the transition points between "1" (high) and "0" (low) of data bits of a received data pulse stream from the transmission line and generates width variable pulse at the detected position, a tank circuit 20 which extracts a timing wave of the data pulse stream from the circuit 10, and a square wave transforming circuit 30 which outputs timing clock synchronous to the timing wave. The decision circuit comprises a D-type flip-flop 40.

In the regenerator shown in FIG. 2, the transition detect and pulse generating circuit 10 is connected to the input side of the tank circuit, and no phase adjuster as used in the prior art is connected between the clock input of the D-type flip-flop 40 and the square wave transforming circuit 20. An input terminal 1 is assumed to accept a data pulse stream of 100 Mbit/s which are encoded in NRZ (non-return to zero) format. The received data pulse stream is fed into the transition detect and pulse generating circuit 10 and the data input terminal of D-type flip-flop 40.

An input buffer amplifier 11 supplies a non-inverted version of the received data pulse stream ((a) in Fig. 3) to one of the input terminals of an exclusive OR gate (EX-OR) 12 and an inverted version ((b) in Fig. 3) to a delay circuit 13. Responsive to the output of the buffer amplifier 11 and a delayed pulse stream ((c) in Fig. 3) from the delay circuit 13, the EX-OR gate 12 generates a stream of pulses of the width τ ((d) in Fig. 3) which is determined by the delay time τ of the delay circuit 13. The pulse stream ((d)) from the EX-OR gate 12 is supplied to the tank circuit 20 via a resistor 17 and a capacitor 18. Resistors 14, 15, and 16 are termination resistors and are connected to a termination voltage source (V_T) at one terminal thereof.

The tank circuit 20 is a bandpass filter which has a center frequency of 100 MHz in passband, and extracts a timing wave of the received data pulse stream out of the output signal of the EX-OR gate. The transforming circuit 30 amplifies the timing wave of 100 MHz and transforms it to a clock pulse stream ((f) in Fig. 3) in synchronization with the timing wave. The clock pulse stream is fed to the clock input terminal of the D-type flip-flop 40 and a buffer 50, and then outputted from the buffer 50 to other processing circuits.

The phase of the output signal from the tank circuit 20 can be changed in proportion to the pulse width τ of the pulses generated from the EX-OR gate 12. By way of example, assume the received data pulse stream alternately repeats in pulse "1" and "0" in NRZ format as shown in FIG. 4. The EX-OR gate 12 outputs a stream i(t) of pulses having the width τ and period T_1. The periodic pulse stream i(t) is expanded in Fourier series as follows:

$$i(t) = \tau/T_1 - (1/n\tau) \cdot \sum_{n=1}^{\infty} \left\{\cos(2\pi n\tau/T_1) \cdot \sin(2\pi nt/T_1) - \sin(2\pi nt/T_1) - \sin(2\pi n\tau/T_1) \cdot \cos(2\pi nt/T_1)\right\}$$

The expression can be transformed further as below:

$$i(t) = \tau/T_1 - (1/n\tau) \cdot \sum_{n=1}^{\infty} \left[2 \cdot \sin(-\pi n\tau) \cdot \cos\left\{(2\pi n/T_1) \cdot (t - \tau/2)\right\}\right]$$

This equation indicates that each frequency component becomes delayed by $\tau/2$ in responsive to the pulse width τ. As the tank circuit 20 extracts the fundamental frequency component of the pulse stream i(t), the phase of the timing wave from the tank circuit 20 can be delayed by $\tau/2$ in proportion to the pulse width τ.

Accordingly, the timing of a clock pulse stream produced in the square wave transforming circuit 30 can be set by adjusting the pulse width τ which is determined by the delay τ of the delay circuit 13. Thus, the clock pulses can be fed directly to the D-type flip-flop 40 through no phase adjuster which limits passband once the clock pulses are recovered. Such clock pulses drive the flip-flop and sample the received data pulse stream with appropriate timing to produce a regenerated data pulse stream. Thus, the present invention provides a stable and accurate timing discrimination in the regenerator.

In FIG. 2, the delay circuit 13 may be any of a gate logic IC, coaxial cables, or strip lines, while the square wave transforming circuit 30 may be a limitting amplifier, a comparator or other high-speed analog circuits.

The data pulse stream is not limited to a NRZ format but may be other ones such as a CMI (coded mark inversion) format. However, unlike NRZ format, CMI format includes a code of two bits per one time slot. Therefore, when a CMI signal is received, the tank circuit 20 extracts a timing wave of the frequency twice as much as the NRZ signal so as to allow detection of the "1" or "0" status within one time slot.

As described in detail in the foregoing statement, this invention can effectively adjust the discriminating timing of "1" and "0" of a received data pulse stream by simply changing the width of the pulses generating at

the transition point of the received data pulse stream and extracting a timing waves.

Claims

1. In a digital signal regenerator responsive to a data bit stream having a predetermined bit rate for generating a retimed data bit stream, the digital siganal regenerator comprising:
transition detect and pulse generating means responsive to the data bit stream for detecting transition positions between two different states of the data bit stream and for generating width variable pulses at the transition positions;
filtering means responsive to the width variable pulses for extracting a timing wave of the data bit stream;
clock pulse generating means responsive to said timing wave for generating a clock pulse sequence; and
discriminating means responsive to the clock pulse sequence for discriminating the levels "1" and "0" of the data bit sequence to generate the retimed data bit stream.

2. The digital siganl regenerator as claimed in Claim 1, wherein the timing pulses of the clock pulse sequence is adjusted by a pulse width of the width variable pulses.

3. The digital signal regenerator as claimed in Claim 1 characterized wherein the transition defect and pulse generating means comprises inverting means for inverting the data bit stream to produce an inverted data bit stream, delay means for delaying said inverted data bit stream to generate a delayed data bit stream, and an exclusive OR circuit means responsive to the data bit stream and the delayed data bit stream for generating the width variable pulses.

4. The digital signal regenerator as claimed in Claim 1 wherein the data bit stream is encoded into a non-return-to zero (NRZ) format.

5. In a timing recovery circuit responsive to a data bit stream having a predetermined bit rate for recovering the timing of the data bit stream, the timing recovery circuit comprising:
transition detect and pulse generating means responsive to the data bit stream for detecting transition positions between two different states of the data bit stream and for generating width variable pulses at the transition positions;
filtering means responsive to the width variable pulses for extracting a timing wave of the data bit stream; and
clock pulse generating means responsive to said timing wave for generating a clock pulse sequence.

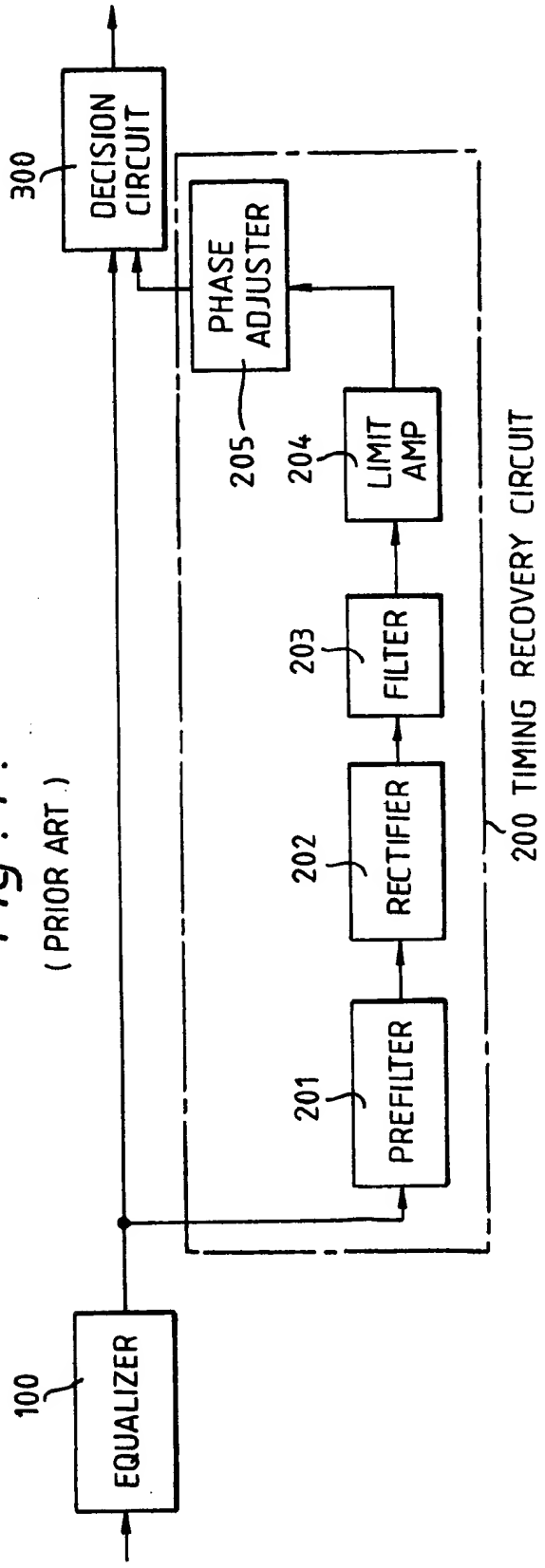


Fig. 1.
(PRIOR ART)

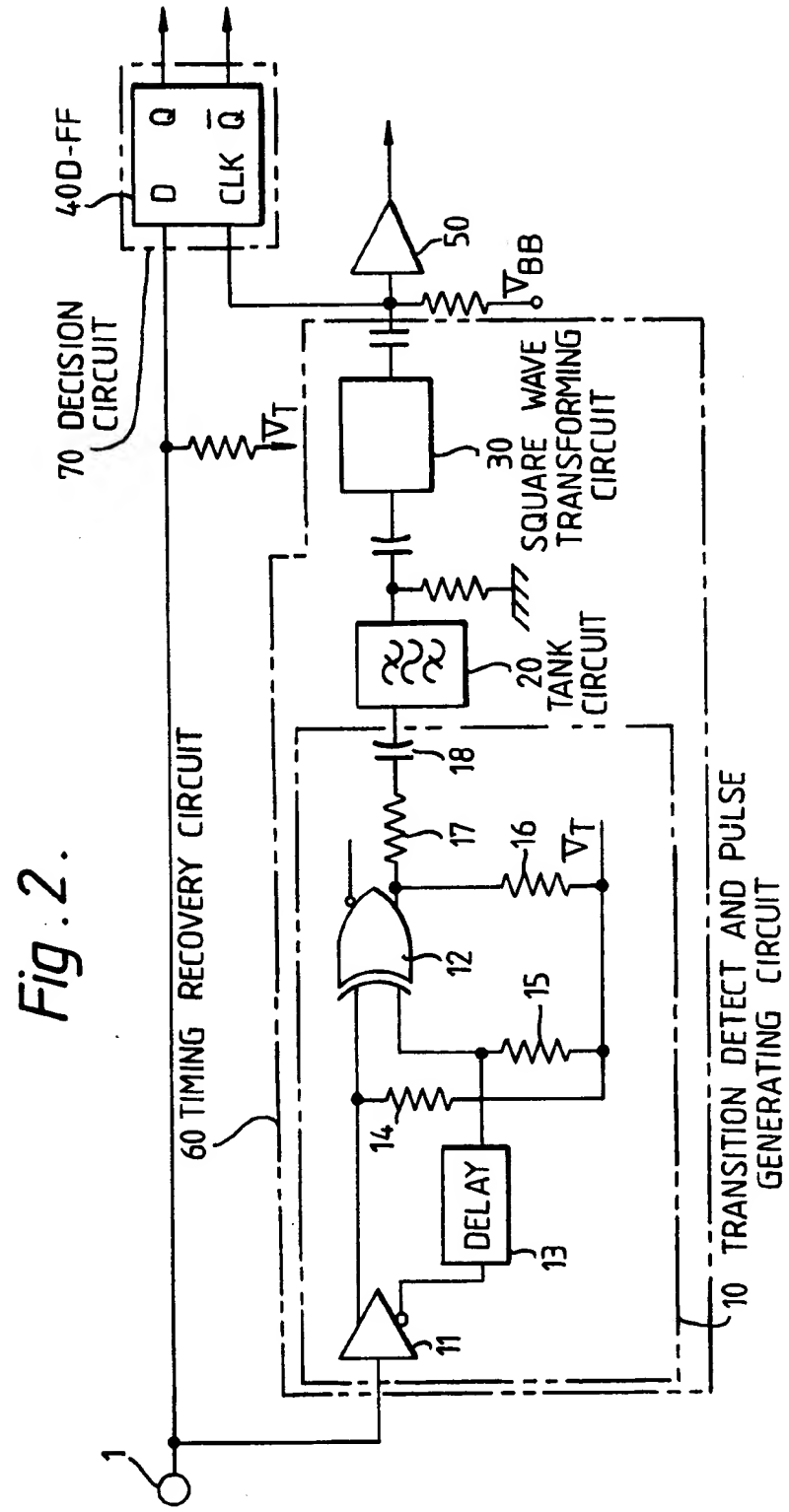
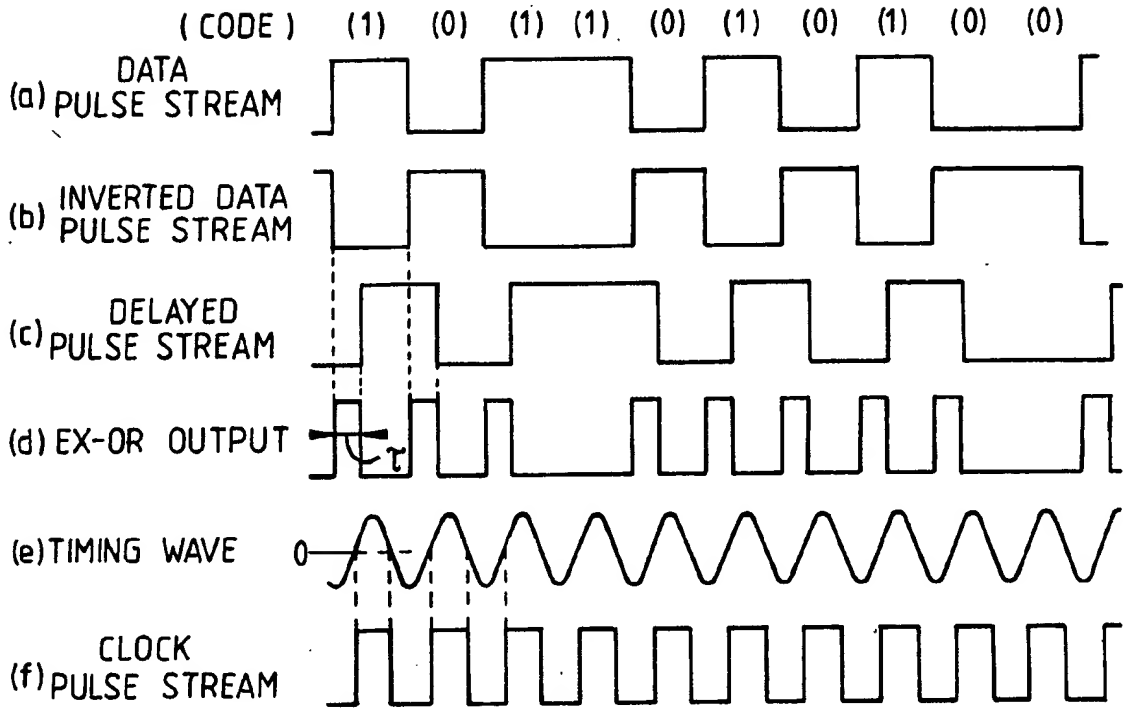

40D-FF
D
Q
CLK
$\bar{Q}$
70 DECISION CIRCUIT
50
V_{BB}
V_T
30 SQUARE WAVE TRANSFORMING CIRCUIT
20 TANK CIRCUIT
18
17
16
V_T
12
15
14
DELAY
13
11
60 TIMING RECOVERY CIRCUIT
10 TRANSITION DETECT AND PULSE GENERATING CIRCUIT
1

Fig. 2.

Fig. 3.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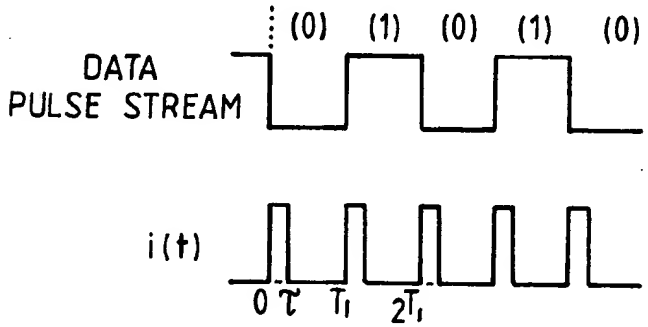
(0)
(a) DATA PULSE STREAM
(b) INVERTED DATA PULSE STREAM
(c) DELAYED PULSE STREAM
(d) EX-OR OUTPUT
τ
(e) TIMING WAVE
0
(f) CLOCK PULSE STREAM

Fig. 4.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DATA PULSE STREAM
i(t)
0
τ
T1
2T1